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SOI Substrate Removal for SEE Characterization: Techniques and Applications

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***Abstract*—Techniques for removing the back substrate of SOI devices are described for both packaged devices and devices at the die level. The use of these techniques for microbeam, heavy-ion, and laser testing are illustrated.**

***Index Terms* - Substrate removal, laser testing, heavy-ion testing, microbeam testing**

I. Introduction

The thick overlayers of today's IC technologies make laser and low-energy heavy-ion and proton SEE characterization from the frontside problematic. For example, the overlayers can attenuate the low-energy ions incident on an IC during ion microbeam SEU characterization. This is especially true for advanced IC technologies that can utilize many layers of metallization. Flip-chip packaging can also limit access to the top side of the die and make SEU characterization extremely difficult. Indeed, several techniques have been developed to thin bulk silicon devices for backside irradiation or to improve their SEU response, including mechanical lapping, chemical etching, and laser ablation [1]–[4]. Recently, work has been performed investigating SEE and charge collection on silicon-on-insulator (SOI) devices with the back substrate removed [5]–[8]. Even though techniques for etching the substrates have been outlined, there are numerous practical issues that must be overcome to successfully etch devices without degrading their electrical characteristics.

We have been exploring a variety of techniques to remove the back substrate of SOI devices. In this work, we describe different techniques for removing the back substrates. Techniques applicable to packaged parts and IC die are described. Lessons learned and the benefits and tradeoffs of the different techniques are discussed. Techniques found to reliably remove the back silicon substrate and techniques that did not work as well will be described. In addition, the advantages of removing the back substrate for SEE characterization are illustrated using microbeam measurements.

II. General Experimental Details

In all cases, the back substrates were removed down to the buried oxide using a XeF_2 etch, as was done in previous work [5], [6]. Prior to etching, the tops of the die were coated with a thick non-conducting epoxy or plastic material to give the etched devices structural integrity once the silicon substrates were removed. The silicon etch was performed using an XACTIX e1 series XeF_2 etch tool. This tool uses vapor phase XeF_2 to selectively etch silicon compared to silicon dioxide. The silicon etch rate was approximately 5 μm per minute with a selectivity to the buried silicon dioxide of approximately 500:1. This silicon etch rate is load dependent and varies based on the sample size. Prior to etching the silicon, it is important to remove any oxide on the surface of the silicon. This can be done by using a reactive ion etch consisting of a 60 second oxygen clean followed by a 60 second oxide etch.

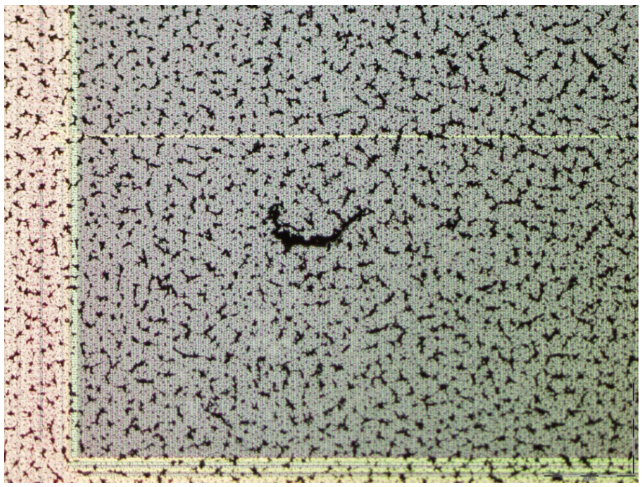

Fig. 1. Residual contamination remaining on buried oxide after silicon substrate has been removed using a a XeF_2 etch. EDS analysis was used to identify the contamination as having a large concentration of gold.

During the initial XeF_2 etch process development cycle, it was found that a significant amount of residual contamination was being left behind on the buried oxide surface as shown in Figure 1. Energy-dispersive x-ray spectroscopy (EDS) analysis showed that this residual contamination had a high concentration of gold. It was speculated that this gold came from exposed gold on the packages or PC boards (from the metal leads and traces) that was being sputtered onto the etched areas, leaving behind large areas of contamination on the buried oxide of the ICs. This gold contamination was mitigated by covering all surface areas (except the areas to be etched) as much as practical with kapton tape. With the kapton tape, no gold contamination was observed. Another issue is that the XeF_2 etch tends to etch from the outside of

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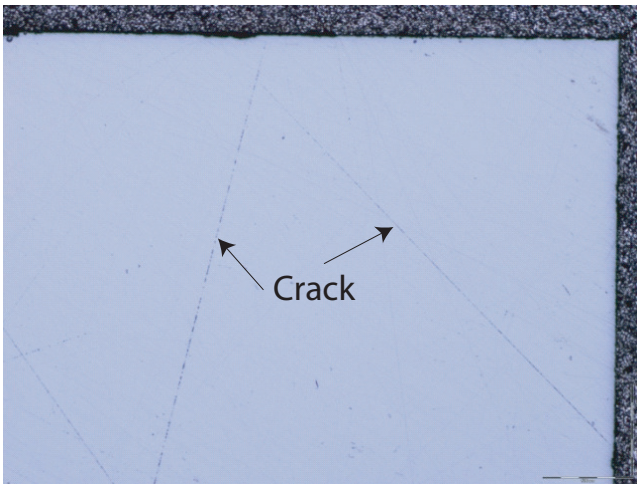

Fig. 2. Back substrate after grinding and before substrate removal.

the die to the center. Care must be taken to develop a XeF_2 etch process with a high Si to SiO_2 selectivity to ensure the etch does not go through the oxide at the edges of the die before all the Si substrate is removed from the center of the die. Some type of residual material can also remain on the buried oxide surface after etching. The cause and nature of this residual material is presently not known. However, based on initial test results it does not appear that this residual material is thick enough to affect laser, heavy-ion broadbeam, or microbeam characterization.

The devices used in this work were fabricated in Sandia's CMOS7 0.35-μm radiation-hardened SOI technology. Prior to etching, the back silicon substrate thickness is 675 μm, the top silicon layer thickness (before device processing) is 270 nm, and the buried oxide thickness is 200 nm. Several types of devices were used to evaluate the etching techniques, including both diodes and ICs. The diodes were specially designed large area didoes for charge collection studies. There are four diodes on a test die and each diode has an area of 600 $\times$ 600 μm^2. Several different types of ICs were etched. They include a 1-Mbit SRAM, a dual port SRAM, and D-flip-flop test structures. Most of these ICs have relatively large areas. For example, the 1-Mbit SRAM has an area of 8.9 $\times$ 9.3 mm^2.

III. Techniques for Packaged Devices

Several combinations of etching, packaging, grinding and polishing were explored for removing the back substrate. In one approach, devices were first mounted in DIP packages with the active area of the IC facing up. The top package cavity was then filled with non-conducting epoxy. The backs of the packages were then mechanically ground and polished to expose the back silicon substrates. Note that the grinding and polishing process also removes part of the package itself. For the DIP packages used in this work, approximately half of the package was removed by the grinding and polishing process. After exposing the back substrates, the back substrates were removed using the XeF_2 etch. The etched packages were then soldered to PC boards.

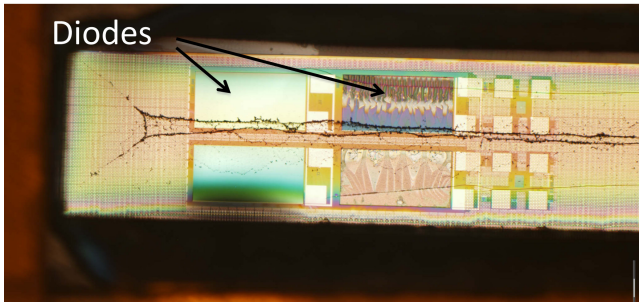

Fig. 3. Photograph of the diodes after removal of the back substrate using the mechanical grinding/polishing process.

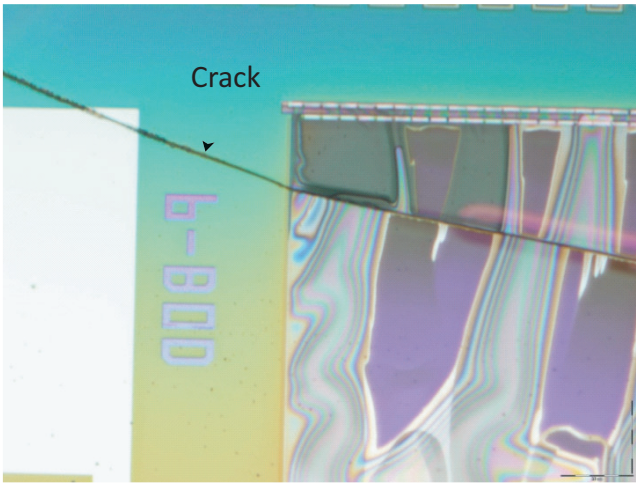

Fig. 4. Back surface after grinding and substrate removal.

In theory, this procedure should be ideal for preparing commercial ICs, including ball grid array ICs, for backside characterization. However, several problems were encountered with this procedure. Figure 2 is a photograph of the back surface of an IC after mechanical grinding and polishing. After the mechanical grinding and polishing process used to expose the backside of the die, very thin microcracks were observed on the back substrates (Figure 2). It is believed that these microcracks were introduced during the mechanical grinding and polishing process (no cracks were observed on die that had not been ground and polished). When the back substrates were removed by the XeF_2 etch, it was found that the active silicon islands were removed. This could be the result of significant over etching along the cracks.

Figure 3 is a photograph of a section of the die after removal of the back substrate. The photograph shows four diodes. Two of the diodes were functionally good with no apparent damage to the diodes. These two diodes are the diodes on the left side of the photograph. The images of these diodes reveal very smooth surfaces, as should be observed if the silicon etch evenly removed the back substrate. The other two diodes on the right side of the photograph were non functional (open circuits). The images of these diodes reveal non-uniform patterns on the back surface indicating a very non-uniform etching process. A magnified image of a section of these diodes is given in Figure 4. Top and bottom photographs of

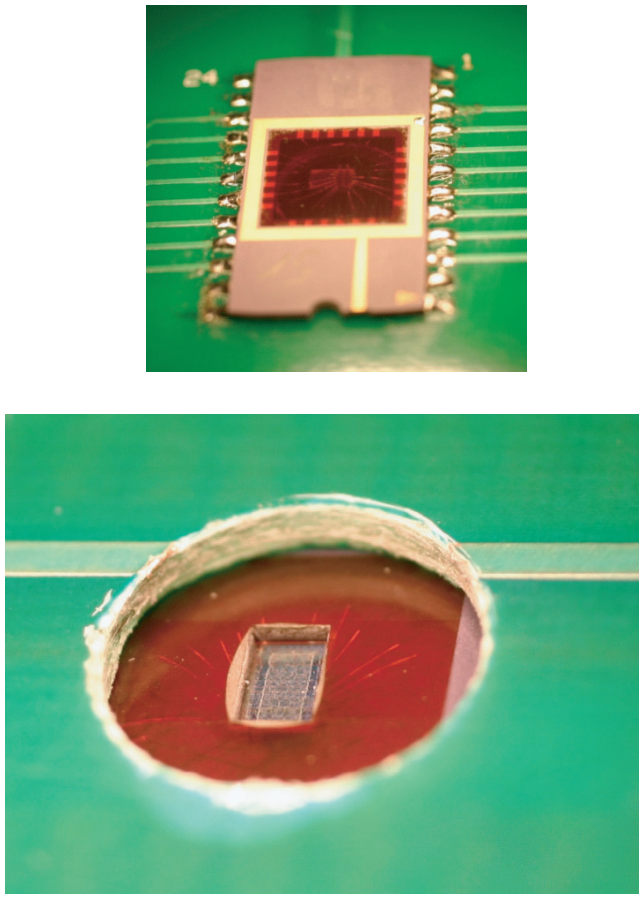

Fig. 5. The top photo shows a mechanically ground package attached to a PC board for testing. The bottom photo shows the back surface after grinding the package and substrate removal with XeF_2.

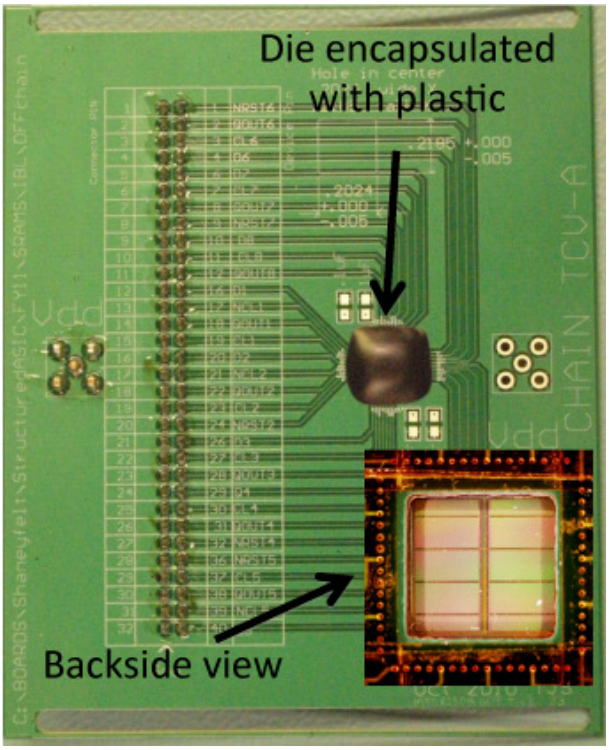

Fig. 6. Frontside and backside view of PC board with attached die. Board is designed to be compatible with XeF_2etch chamber and microbeam, laser, and heavy-ion testing.

the PC board with the mechanically ground package attached with the back silicon etched are displayed in Figure 5. Another possible problem with this process is thermal stress during attachment of the thinned packages (approximately one-half their original thickness) to PC boards. The thermal stress could potentially cause cracking of the thinned substrates. This effect can be reduced by minimizing the temperature increase of the packages during soldering.

IV. Techniques When Die Are Available

In another approach, the backs of the packages were first milled and then back-side polished die were epoxy bonded to the milled packages. After that, the tops of the packages were filled with non-conducting epoxy and the back substrates were etched in XeF_2. The front and backsides of the package were covered with kapton tape to protect gold traces to minimize gold contamination of the etch chamber. These packages were then mounted on PC boards, which also had holes milled out to expose the back surfaces of the devices. This approach avoided problems with cracking associated with the grinding process. There were no apparent deleterious effects of this approach on the electrical performance of ICs [5].

In a third approach, a PC board was designed with a pre-cut hole that exposes the backside of the die. The board was designed to be compatible with laser testing, heavy-ion broadbeam testing, and microbeam testing. Of course, the PC board also had to fit in the etch chamber. Die were then directly attached to the PC boards, wire bonded, and then encapsulated with non-conductive plastic material. The back of the substrates were then etched in XeF_2 down to the buried oxide. The front and backsides of the PC boards were were covered with kapton tape to protect gold traces and to minimize gold contamination of the etch chamber. As a final step, electrical connectors can then be attached to the PC board. Figure 6 is a photograph of a finished PC board, with the inset showing the etched die from the backside. This process works very well when die are available. Fully functional, large area ICs can be etched in this manner.

V. Applications

Removing the back substrate has proven to be extremely useful for backside SEE characterization using a single-photon absorption (SPA) laser technique and heavy-ion broadbeam characterizations of ICs [5]–[8]. We have also applied it to heavy-ion microbeam characterizations. Figure 7 is an example of a single-event upset map for a 1-Mbit SRAM taken using Cu ions at Sandia's microbeam facility from the backside of the IC with silicon subsrate removed. For the energies available at this facility and for the number overlayers used in this IC, the microbeam has limited usefulness for frontside irradiation because the ions do not have sufficient energy to penetrate all of the overlayers and the device sensitive volumes. However, for backside characterization with the back

substrate removed, the low energy of the ions is no longer an issue. In fact, the energy can be varied to readily vary the ion LET. In the past for frontside characterizations, the LET could only be changed by changing the type of ion. Lowering the energy of the ion for frontside characterizations was not practical in many instances because the ion energy would be significantly attenuated by the device overlayers. Sensitive areas as determined by laser and microbeam measurements can now be compared without interference from device overlayers. It should however be noted that there can be drawbacks to performing SEE characterizations from the backside. One of these is that for high-energy heavy-ion characterizations, the effects of the generation of high LET secondary particles by nuclear interactions of heavy ions with the high-Z materials in the device overlayers will be considerably less for backside irradiations than for frontside irradiations. For instances where these nuclear are deemed to be important, frontside irradiations should still be performed.

VI. Summary

SEE characterizations from the backside with the back substrate removed offer numerous advantages for laser, heavy-ion broadbeam and heavy-ion microbeam measurements. We have developed several techniques for removing the back substrates of SOI devices. Techniques for removing the back substrates of packaged die and for cases where devices are available in die form are described. There are a number of processing issues that must be addressed to successfully remove the back substrates without adversely affecting the electrical characteristics of the devices. We have illustrated the usefulness of the technique by performing the first single-event upset mapping of an IC from the backside using a focused ion microbeam.

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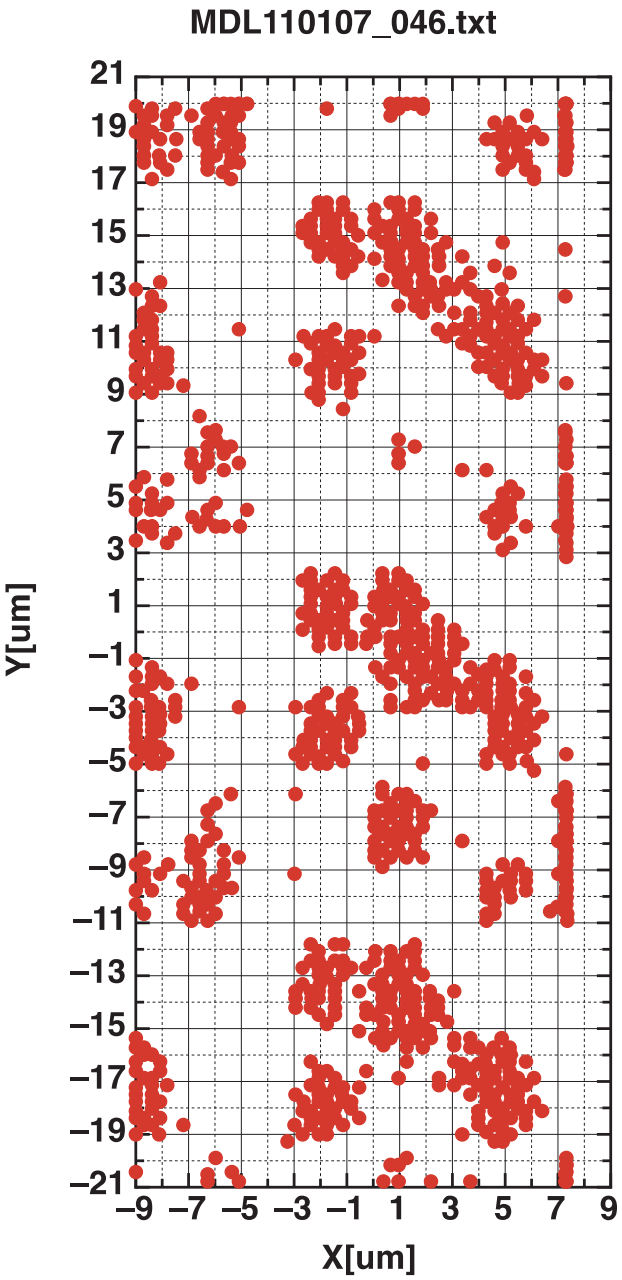

Fig. 7. Single-event upset maps of an IC taken at Sandia's heavy-ion microbeam.

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