cadence®

SPEED2000 Examples 2

Product Version 16.6
December 2012

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Table of Contents

Chapter 1

Introduction

Welcome to ***SPEED2000 Examples2***. This document presents examples of various scenarios you might encounter using the applications. This manual is designed to give you a brief introduction to the application by providing real life examples and demonstrations so you can understand some of the basic concepts of the SPEED2000.

System Requirements

The following system requirements are necessary for SPEED2000:

- Microsoft Windows XP and Windows7
- RedHat Enterprise Linux AS/ES/WS Release 4, x86_64
- RedHat Enterprise Linux AS/ES/WS Release 5, x86_64
- SUSE Linux Enterprise Server 10, x86_64
- Minimum 2GB Memory

How to Use This Guide

The ***SPEED2000 Examples2*** provides demonstration examples and step-by-step instructions on how to get the desired results.

ADDITIONAL DOCUMENTATION

In addition to this document, refer to the following documentation for additional information.

- ***.spd File Format Reference Guide*** details our native .spd file formats.
- ***SPEED2000 Getting Started Guide*** shows you how to start using the functionality in SPEED2000.
- ***SPEED2000 User's Guide*** describes in detail the features and functionality of SPEED2000.

CONVENTIONS USED IN THIS GUIDE

CONVENTION	USE
Bold	GUI text, special names, terms (window names, buttons, menus, etc.)
Arial	Examples
>	Menu hierarchy

HOW TO CONTACT TECHNICAL SUPPORT

If you have questions about SPEED2000, contact the *Cadence Online Support.*

Chapter 2

Examples

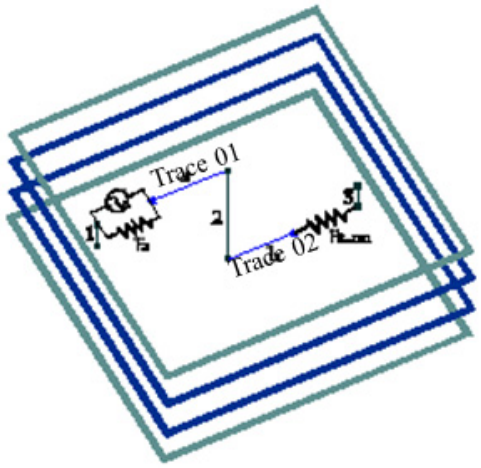
This chapter contains seven examples of various scenarios you might encounter using the SPEED2000 applications.

Example 1 - Power and Ground Voltage Fluctuations

This example contains a package of four metal layers and two simple circuits. The file used in this example is s2k_app1_trace_ref_change.

In the following illustration, the package contains:

- A ground plane
- A signal layer at the bottom
- One power plane
- Signal layer at the top



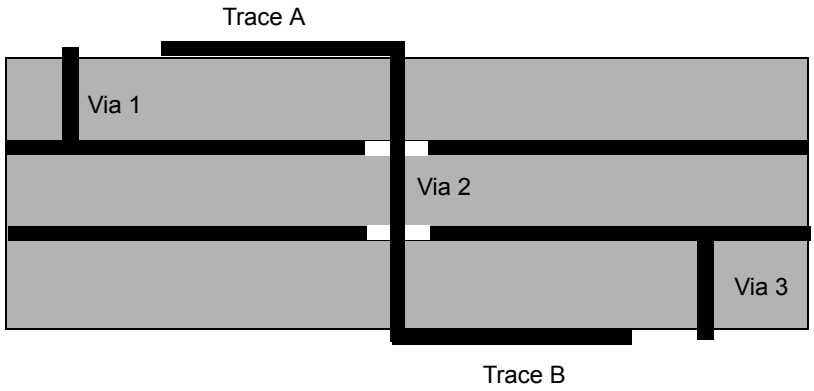
There are two Traces:

- Trace 01 at the top layer and Trace 02 at the bottom signal layer.
- Trace 01 and Trace 02 are connected to each other through Via 2.
- Trace 01 and Via 1 are between the top signal layer and the power plane.

These two Traces are connected in several ways:

- A current source with a source resistor is connected to Trace 01 and Via 1.
- Trace 02 and Via 3 are connected at the bottom signal layer and the ground plane.
- A termination resistor, Rterm, is connected to Trace 02 and Via 3.

Cross-sectional View of the Configuration



The waveform of the current source is a pulse that has:

- 100ps low-to-high transition
- 300ps duration
- 100ps high-to-low transition
- 50 mA in amplitude

SPEED2000 shows you:

- Dynamic spatial distribution of voltage between the power and ground planes.
- Transient current through the current source and flowing into Trace.
- Transient voltages at both the driving end and at the receiving end.
- Transient voltage between the power and ground planes at the center of the package in the window of 2D Curves (Time Variation).

This example demonstrates:

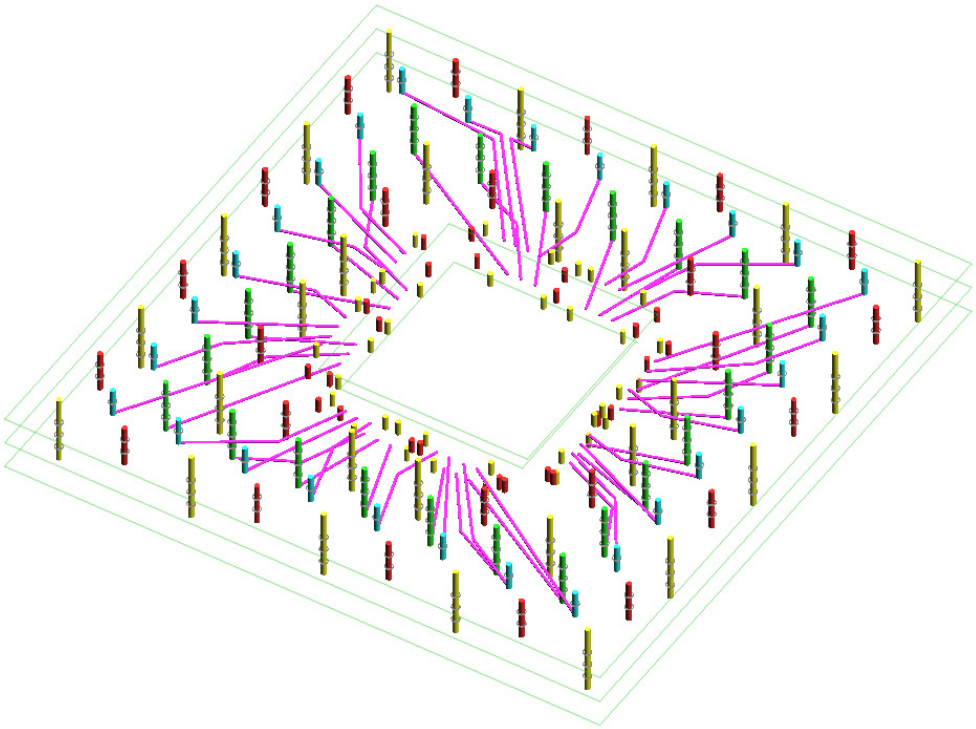
- Power and ground voltage fluctuations are generated by a current in a via passing through two metal planes.
- Noise between metal planes propagates and how it is reflected at the edges of metal planes.

EXAMPLE 2 - POWER / GROUND NOISE AND COUPLING

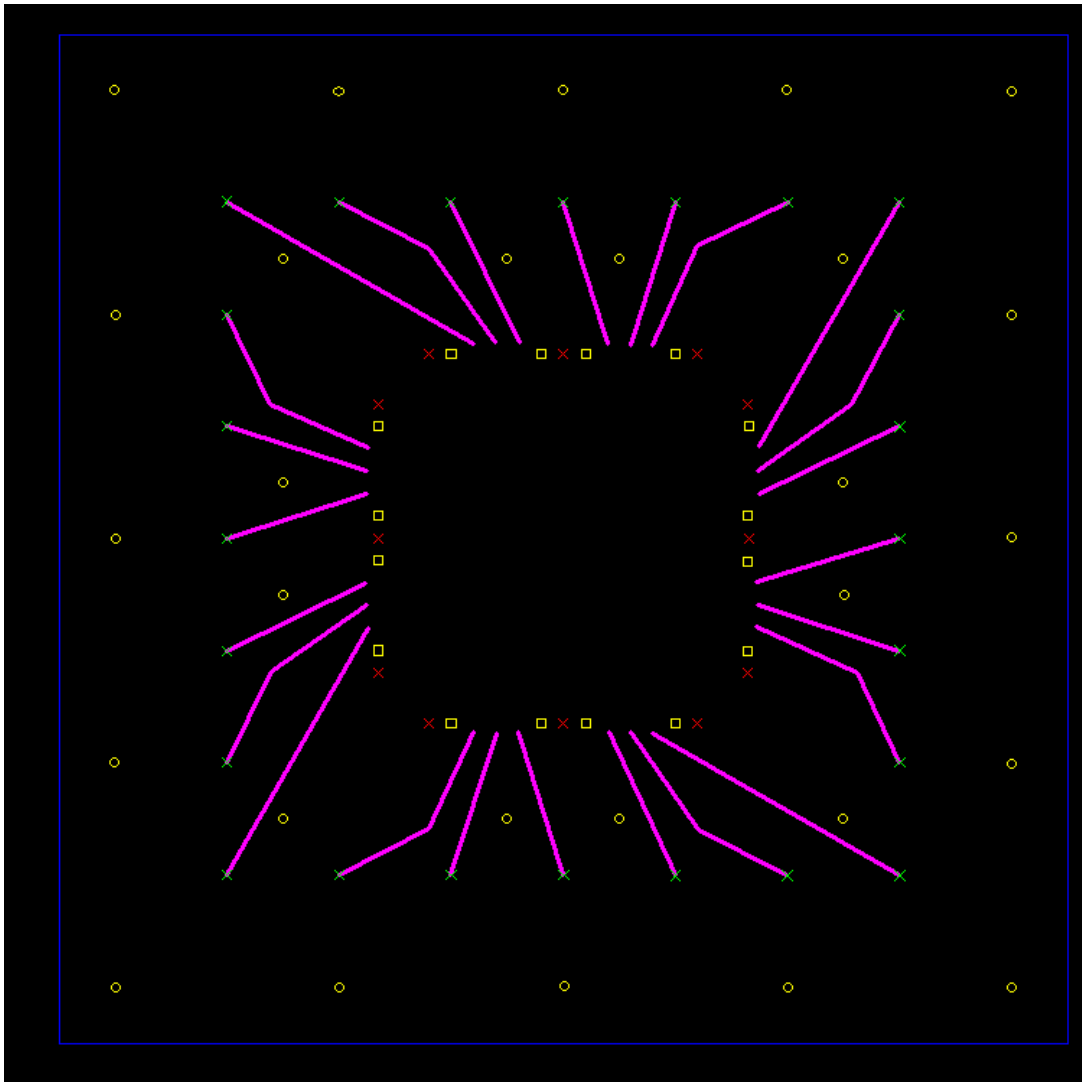
Example 2 uses file s2k_app2_pkg_xtalk.spd. This example shows a chip carrier of 6 metal layers .

- Signal1 and Signal2 are two signal distribution layers,
- Plane1 and Plane3 are ground planes, Plane2 is a power plane.
- Signal3 is the pin layer.

3D Configuration of the IC Chip Carrier

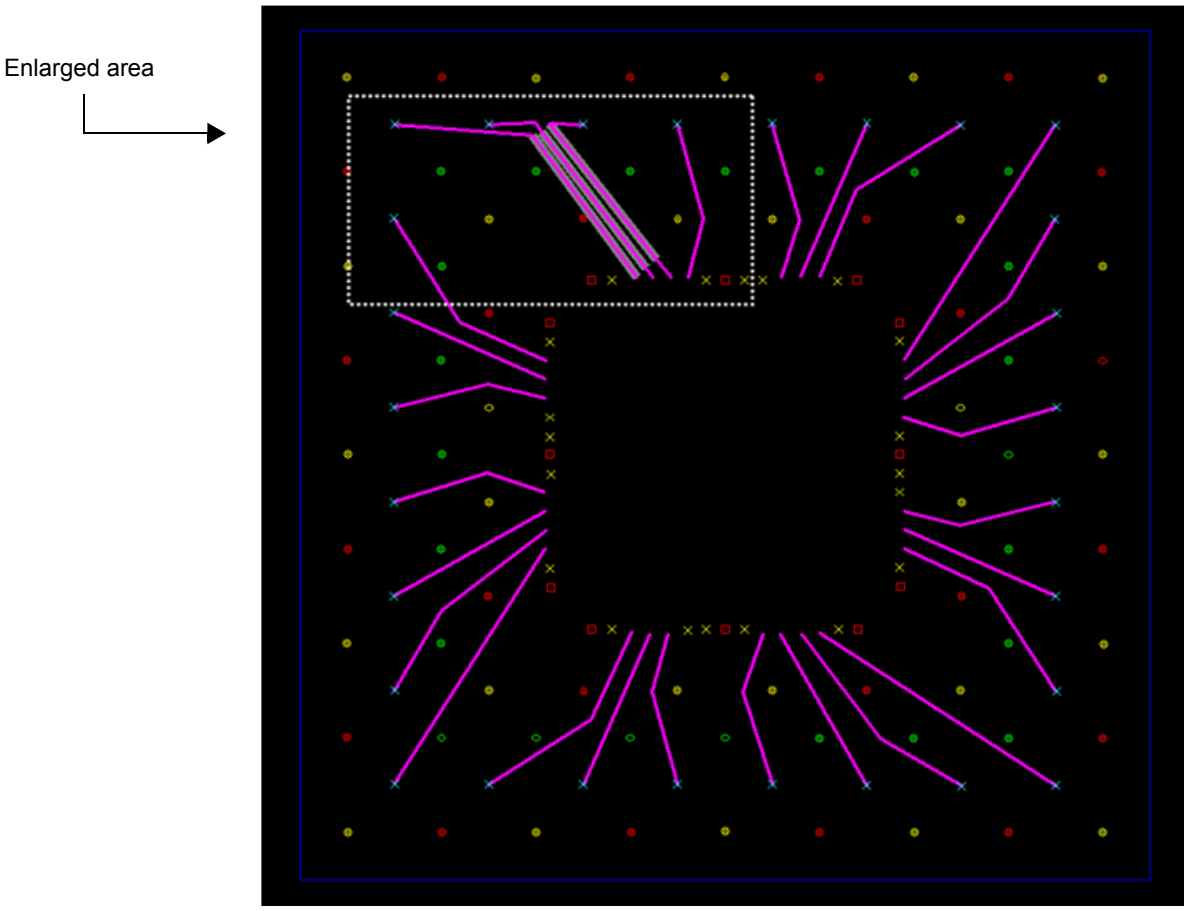


Signal Traces on Layer Signal1



- A driver circuit, consisting of a voltage source with a series resistor, is connected across one end of a Trace and a ground via.
- The waveform of the voltage source is a sine-square pulse of 100 ps rise time, 100 ps duration, 100 ps fall time, and amplitude of 5V.
- The other end of the Trace is terminated by a resister.
- Two signal Traces that are to the left of the active trace are terminated at each end by a resistor.

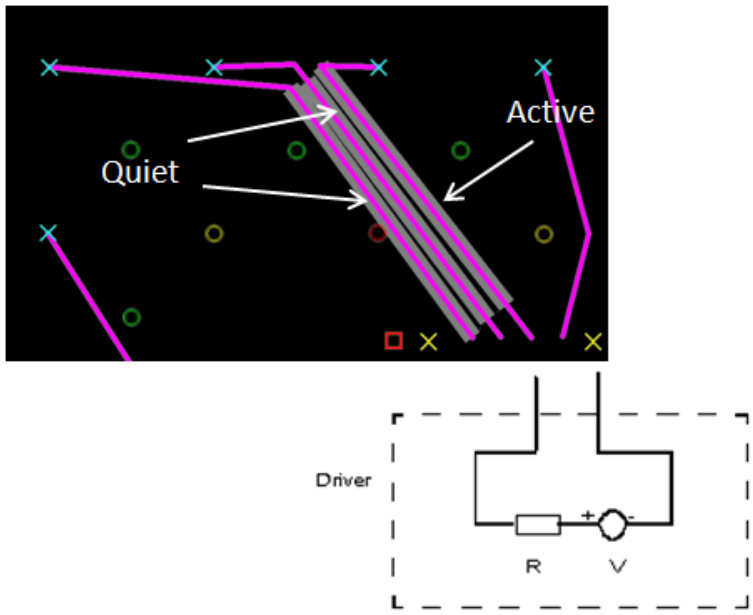
Signal Traces on Layer Signal2



After the simulation starts, you can see:

- In the 3D surface plot window, how the voltage fluctuation between Plane2 and Plane3 initially starts from the location of the excitation source and spreads across the entire plane.
- How the power and ground noise penetrates into the Plane1 and Plane2 layers.
- Near end (V1) and the far end (V5) voltage waveforms of the active Trace.
- Near end (V3) and the far end (V6) voltage waveforms of quiet line1adjacent to the active line.
- Near end (V4) and the far end (V7) voltage waveforms of quiet line2.

Enlarged View of the Upper Left Portion



EXAMPLE 3 - COUPLING BETWEEN VIAS

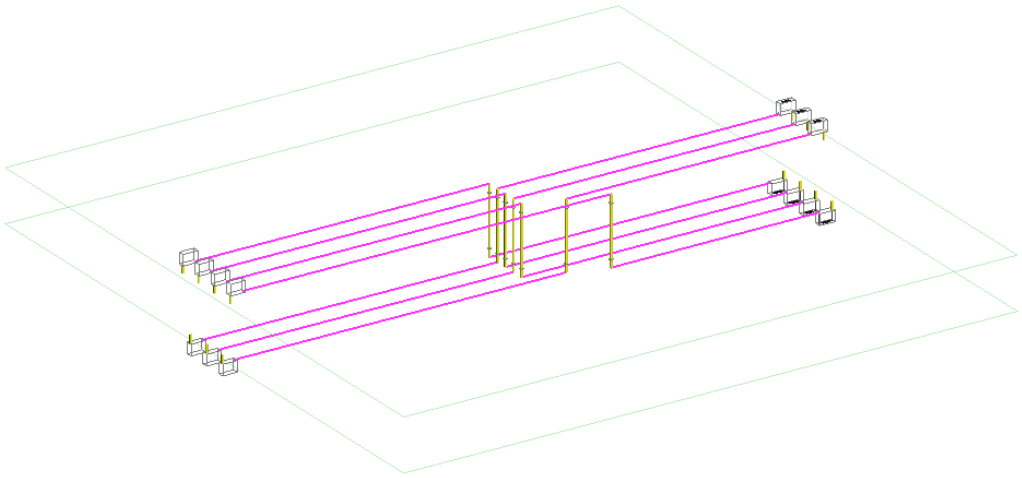
Example 3 shows the coupling between signal nets through vias. The file used is s2k_app3_via_xtalk.spd. The sample illustration shows the four layer Stackup.

- Bottom signal layer
- Top signal layer
- Two metal planes

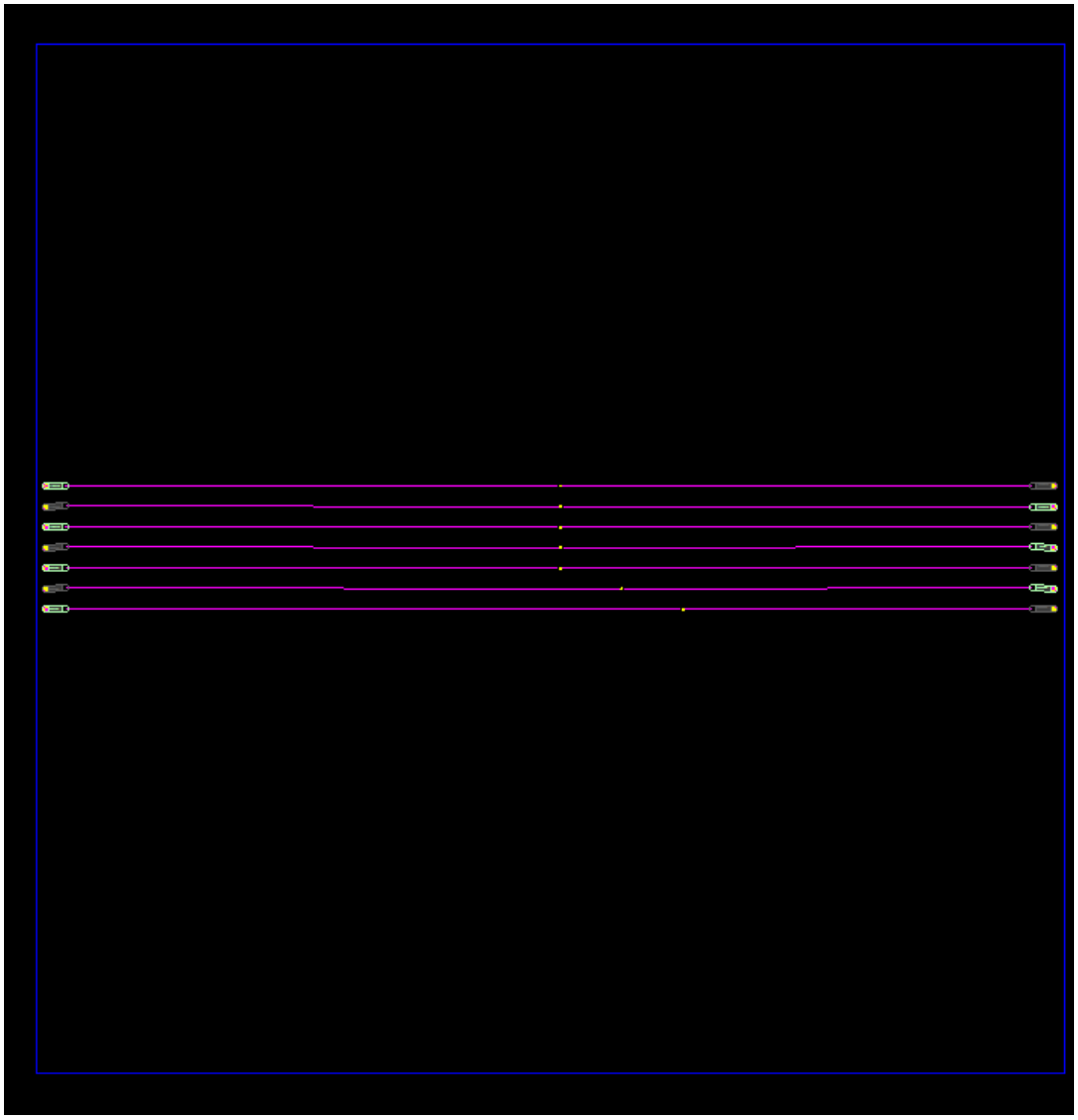
Altogether, there are seven parallel signal nets. Each signal net runs from the top signal layer to the bottom signal layer through a via.

There is one active line, line 4, which is in the middle of the seven lines. All the other six lines are quiet lines. The top view of the structure is shown in the second illustration.

Layers of the Stackup



Top View of the Structure



An excitation source is connected to the right side of the active line. As the current flows through the via of line 4, the fluctuation of voltage between the two metal planes is generated and propagates away from the active via.

As the voltage between the two planes reaches other signal vias, noise voltages are induced in the quiet lines and then propagate towards their end terminals.

From the physical dimensions specified in the file (s2k_app3_via_xtalk.spd), the coupling between parallel Traces is negligible. The noise coupled to quiet lines is dominantly due to the coupling through vias.

Through SPEED2000 simulation, you can see:

- How the voltage between two metal planes is generated at the location of the active via and propagates throughout the plane area;
- Transient voltages at both ends of each of the seven lines.

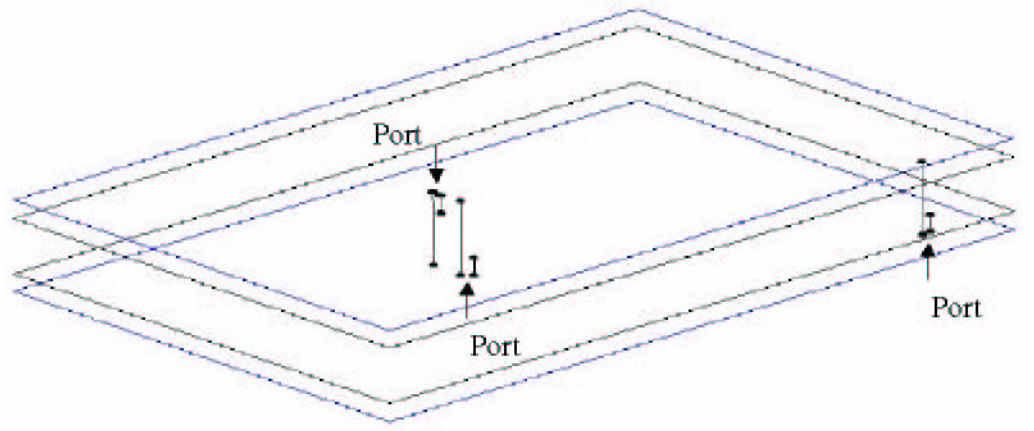
EXAMPLE 4 - EXTRACTION OF S PARAMETERS

Example 4 shows how to use SPEED2000 to extract S-parameters from transient simulation results. The file used in Example 4 is s2k_app4_S-parameter_extract.spd.

The illustration shows the Stackup of the structure:

- Bottom signal layer
- Top signal layer
- Two metal planes

For this example, we want to find S-parameters of the three ports.



Three transient simulations are needed to find three port S parameters. Assume the reference impedances of all the ports are 50 Ohms.

To find S_{j1} (j=1,2, 3), port 1 is connected to a voltage source in series with a 50 Ohms resistor.

- Port 2 and Port 3 are each terminated with a 50 Ohms resistor.
- Waveform of the voltage source is a Gaussian pulse of a pulse width 700 ps, with its spectrum from dc to about 3 GHz.

In transient simulation of SPEED2000, following transient voltages are recorded using a simulation of 200ns:

- V1: Voltage across port 1
- V2: Voltage across port 2
- V3: Voltage across port 3
- V4: Voltage of the voltage source.

After taking the Fourier transforms of the above voltages, S_{j1} (j=1,2, 3) are found as follows:

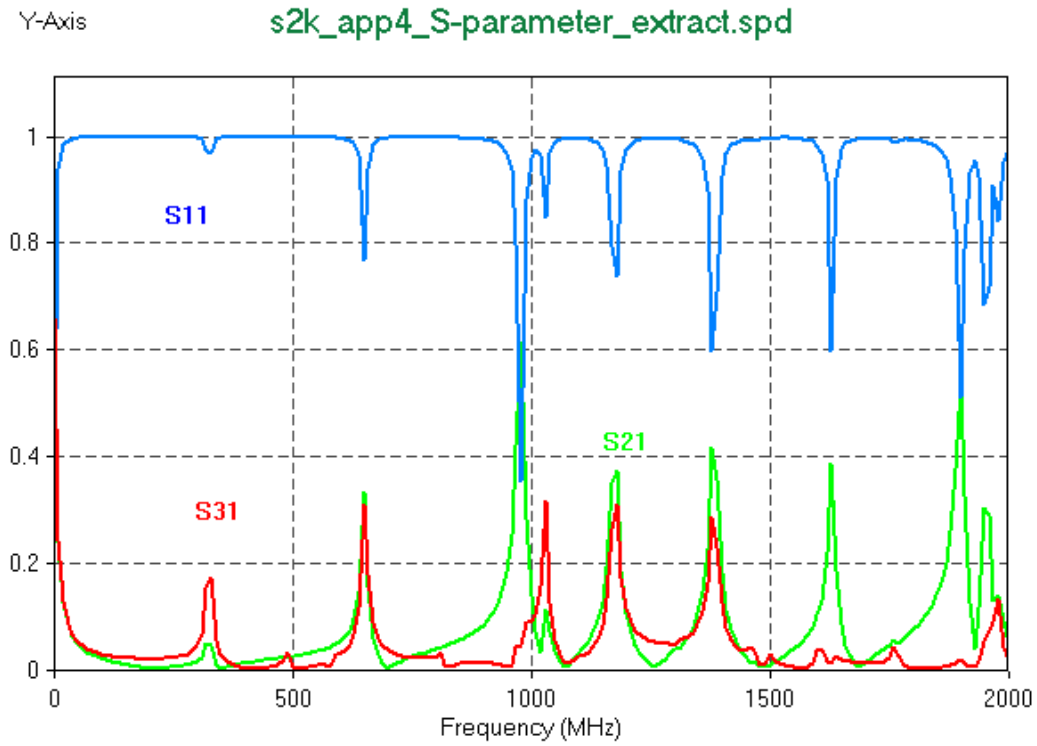
$$S_{11} = \frac{V1(f) - (V4(f))/2}{(V4(f))/2}$$

$$S_{21} = \frac{V2(f)}{(V4(f))/2}$$

$$S_{31} = \frac{V3(f)}{(V4(f))/2}$$

The S-parameters, S_{j1} (j=1,2, 3), obtained from the above procedure are shown in the following screen-shot. Other elements of the S-parameter matrix can be found in the same way.

S11, S21 and S31 of a Three Port System



EXAMPLE 5 - CHARACTERIZATION OF POWER AND GROUND DISTRIBUTION SYSTEM

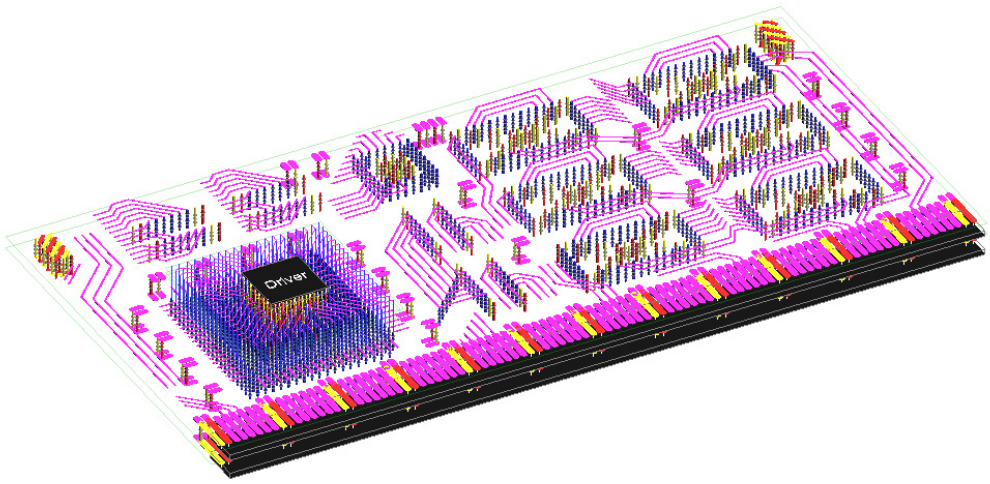
This example contains an 8-layer chip carrier and a 6-layer printed circuit board. The file used for this example is s2k_app5_pkg_board_cosim.spd.

In this example, we want to obtain the input impedance of the power and ground distribution system, looking from the top-layer of the IC chip carrier. An excitation source of the waveform of a Gaussian pulse is used for the characterization.

One end of the source is connected to all the ground nodes on the top layer of the IC chip carrier.

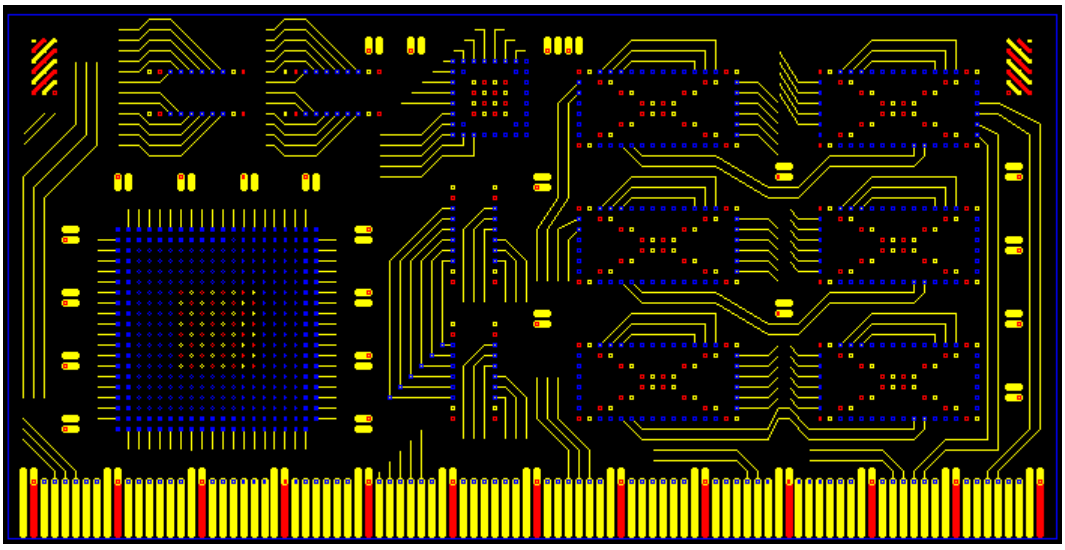
The other end of source is connected to all the power nodes on the top layer of the IC chip carrier.

3D View of the Structure



In the top view of the printed circuit board one can identify footprints of area array and peripheral chip carriers.

Top View of the Printed Circuit Board



During the SPEED2000 simulation, voltage and current are recorded:

- Current (C1) flowing into the package.
- Transient voltage (V1) across the excitation circuit.

After the transient simulation is completed, V1 and C1 are transformed to the frequency domain. The input impedance is calculated by:

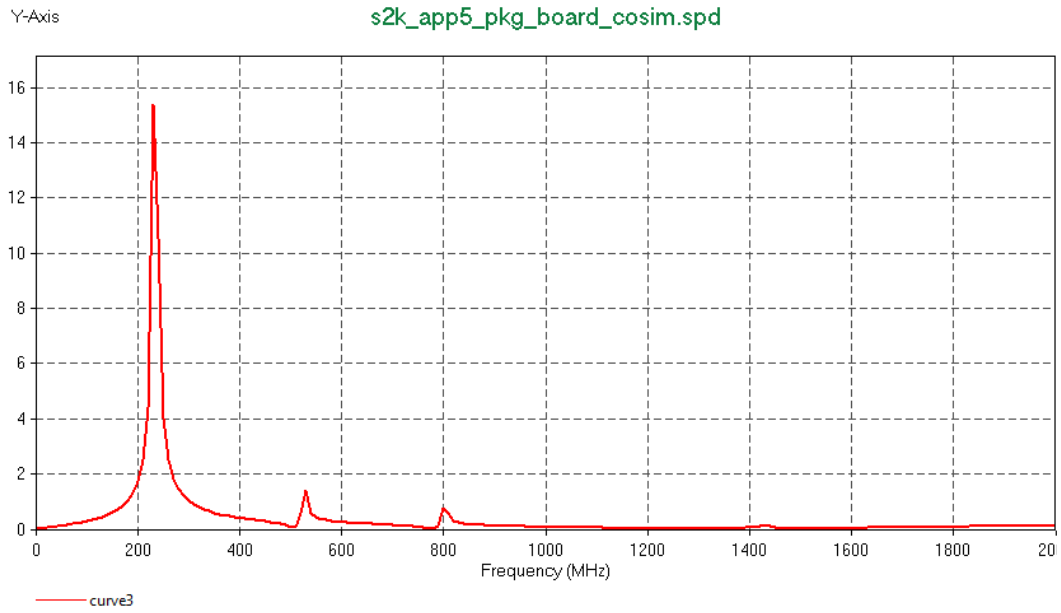
V1(f)/C1(f)

The resonance is apparent from the input impedance curve shown in the next illustration. Notice that

no decoupling capacitors are placed on the board.

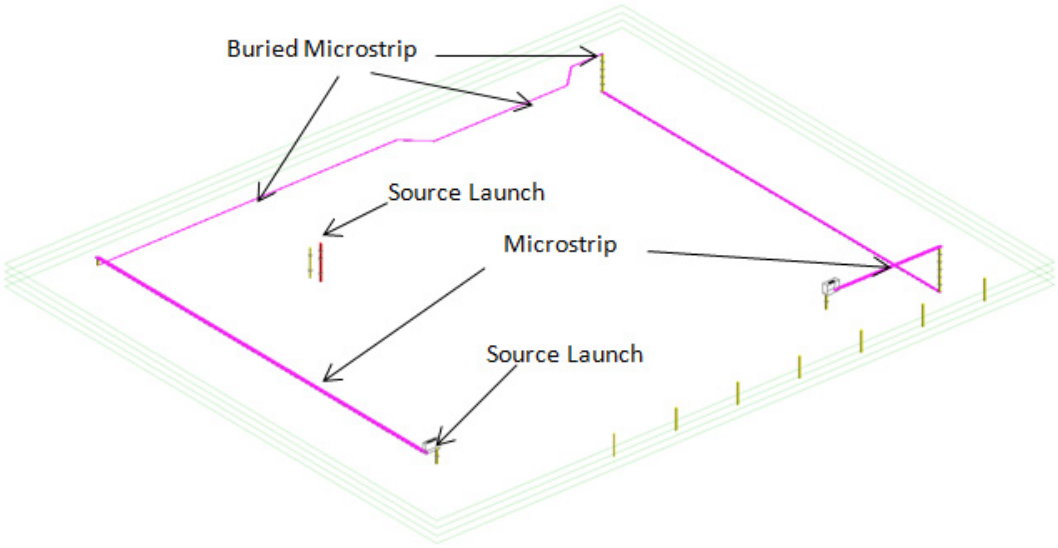
One of the tasks of the power and ground distribution design is to minimize the input impedance of the power and ground system over a specified frequency range.

Input Impedance of the Structure



EXAMPLE 6 - RADIATION FROM PACKAGES

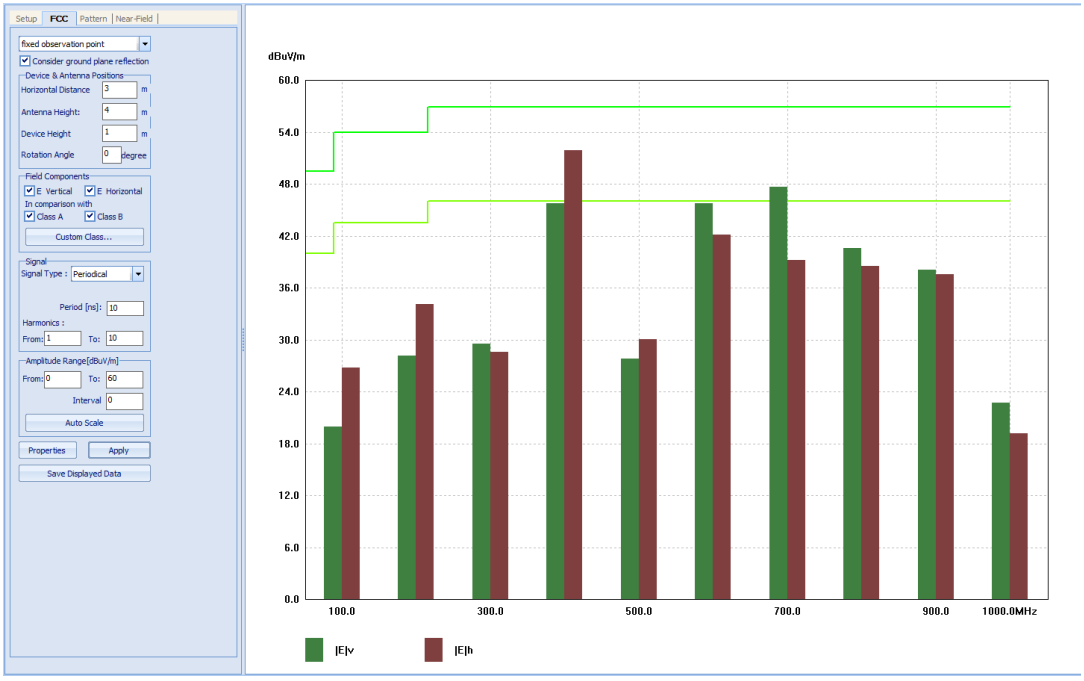
Example 6 uses the file s2k_app6_radiation_clk_ref_change.spd. It shows the 3D configuration of the package. This example demonstrates how to use SPEED2000 to compute radiation from a printed circuit board.



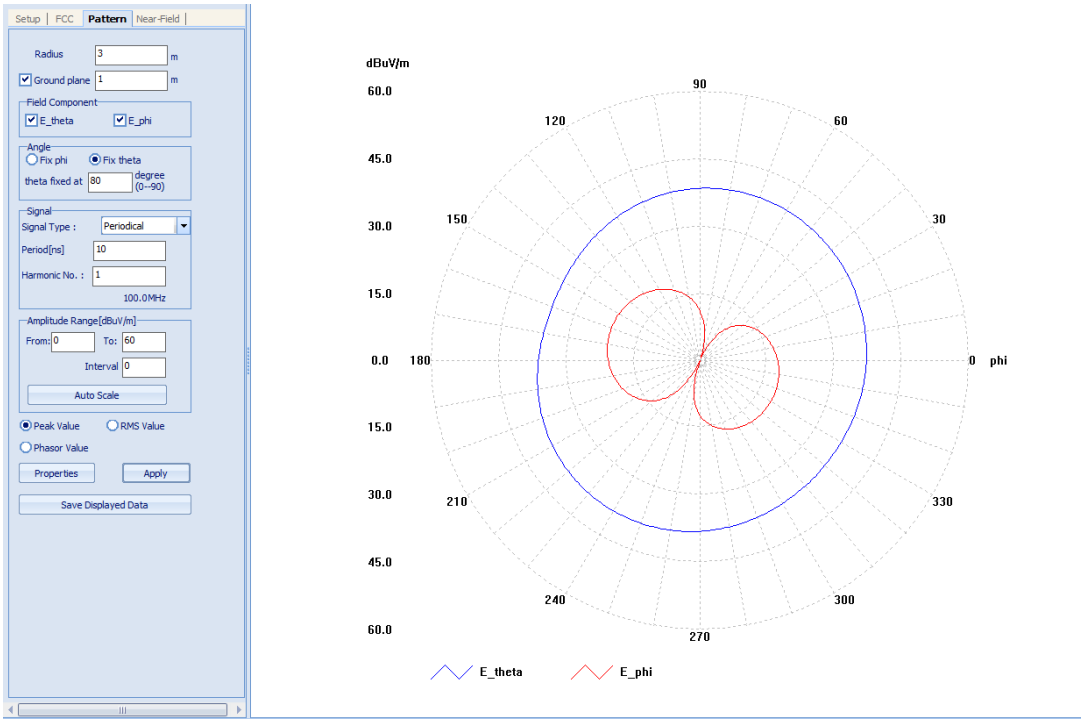
As shown in the next chart:

- One source is connected to the power and ground planes.
- One source is used to represent a driver to a signal net.

SPEED2000 can be used to compute radiation from microstrip and buried microstrip lines, and from edges of metal planes.This illustration shows the radiation from the microstrip and buried microstrip lines, in comparison with FCC regulations.



The last illustration shows the radiation pattern for the radiation from edges of metal planes.



EXAMPLE 7 - EFFECTS OF VIAS ON SIMULTANEOUS SWITCHING AND CAPACITORS

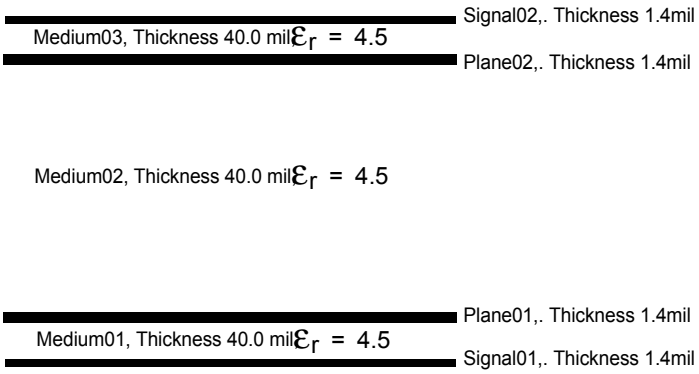
This example demonstrates effects of vias in the case of:

- A large number of buses switching simultaneously.
- The effects of capacitors placed near vias.

The file s2k_app7_sso_decap_study.spd is used in this example.

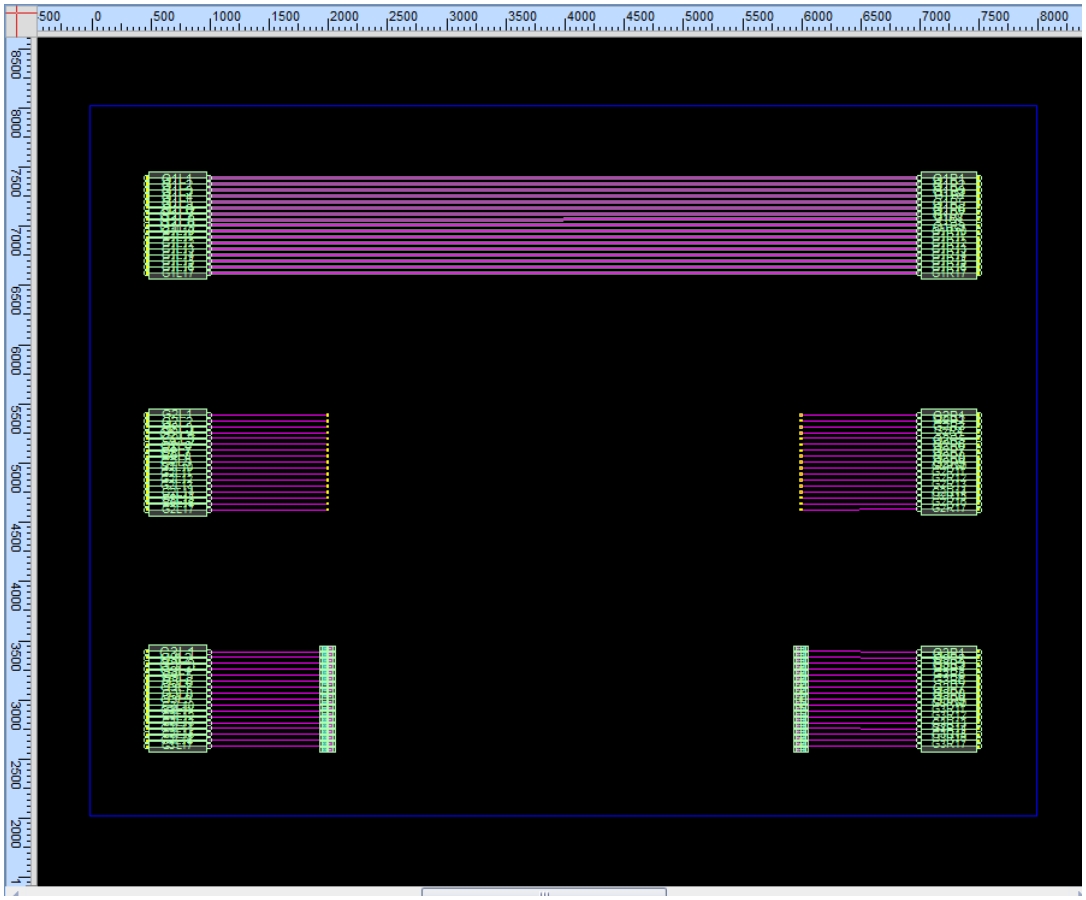
Physical Configurations

Consider a four-layer printed circuit board. The Board Stackup is shown in the next figure.



- Center-to-center separation between adjacent Traces is 50 mils.
- Horizontal dimension of the board is 8 inches x 6 inches.
- Traces are all 16 mils in width and 1.4 mils in thickness.
- Upper and low plane (Plane02, Plane01) have two slots.
- Vias are all 7 mils in radius.

Board Stackup

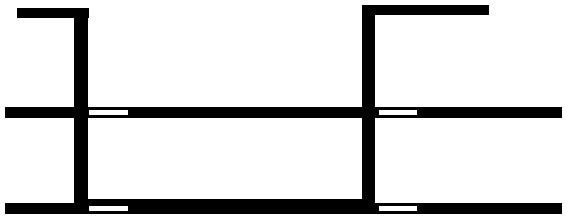


Net Groups

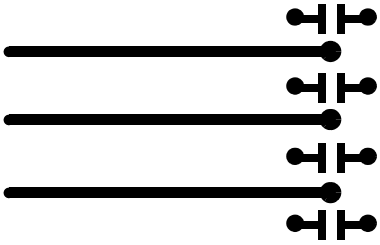
There are three groups of nets in this example. Each group has 17 nets.

- First group of 17 nets is on the top signal layer.
- Second group of 17 nets start from the left end on the top signal layer, passes to the bottom signal layer through vias, then backs to the top signal layers through vias.
- Third group of 17 nets is routed in the same way as that of the second group. In addition, there are total of 72 decoupling capacitors, 36 capacitors for each column of 17 vias.

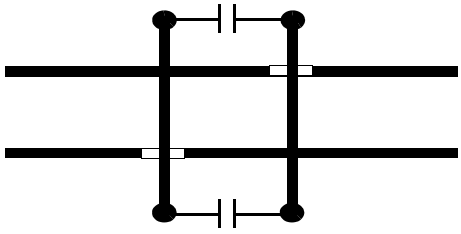
The cross-section of the Trace layout is shown below.



The next figure shows the top-view of capacitors placed near one column of the vias.



There are capacitors mounted on both the top and the bottom signal layers of the board as shown in the last illustration.



Circuit Configuration

Each Trace, without the presence of adjacent Traces, is about 28ohm in its characteristic impedance. When the loss of the transmission line is considered, its characteristic impedance is slightly higher than 28 Ohms.

- Left ends of all nets are each connected to a voltage source in series with a 28 Ohms resistor.
- Right ends of all nets are each terminated by a 28 Ohms resistor.

Near the left edge of the board, each of the three pieces of the upper plane is connected to the lower plane through a 10 mOhms resistor.

The capacitors used are the model 0603 in their dimension. The circuit model of the capacitor is:

C = 47 nF, ESL = 0.9 nH, ESR = 844 mOhms.

- All the nets are driven by the sources simultaneously of the same polarity.
- Amplitude of the voltage source is 2V.
- Waveform of the voltage source is the output of a Bessel filter of a piecewise linear pulse with 300 ps in rise and fall times.

Computation Parameters

A mesh of 320 by 240 is used in SPEED2000 simulation. Each mesh element is of 25 mils x 25 mils. The total simulation time is 10 ns.

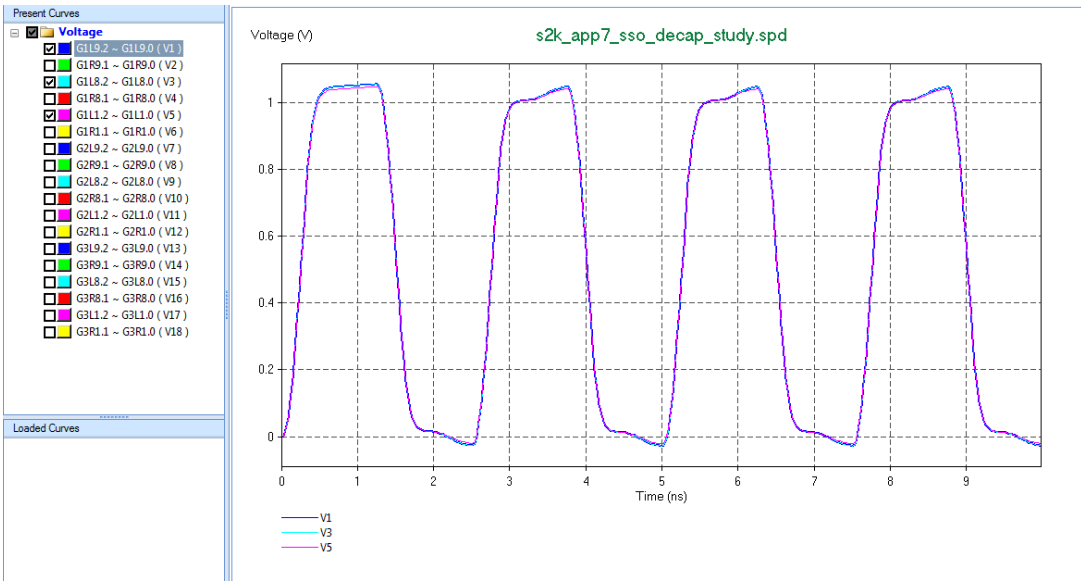
Simulation Results

The first group of 17 nets is considered as 17 coupled transmission lines in the simulation. Voltage waveforms at the source end of the 1st, 8th and 9th nets are displayed in the illustration below in the waveform of the voltage source.

Results of the First Group of Nets

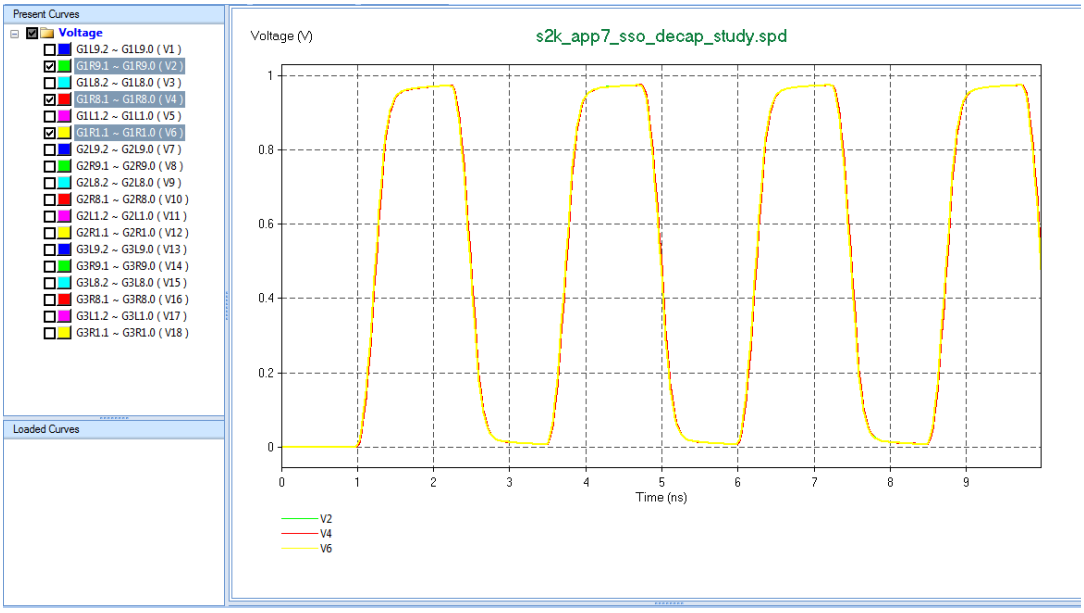
Results of the next two figures imply that, for the configuration of this group of nets, the coupling between adjacent nets is negligible.

The illustration shows the Near End Voltage Waveforms for Group 1. It can be seen that the waveforms of the 8th and 9th nets are almost identical, while that of the 1st net is slightly different from others.



Far End Voltage Waveforms for Group 1

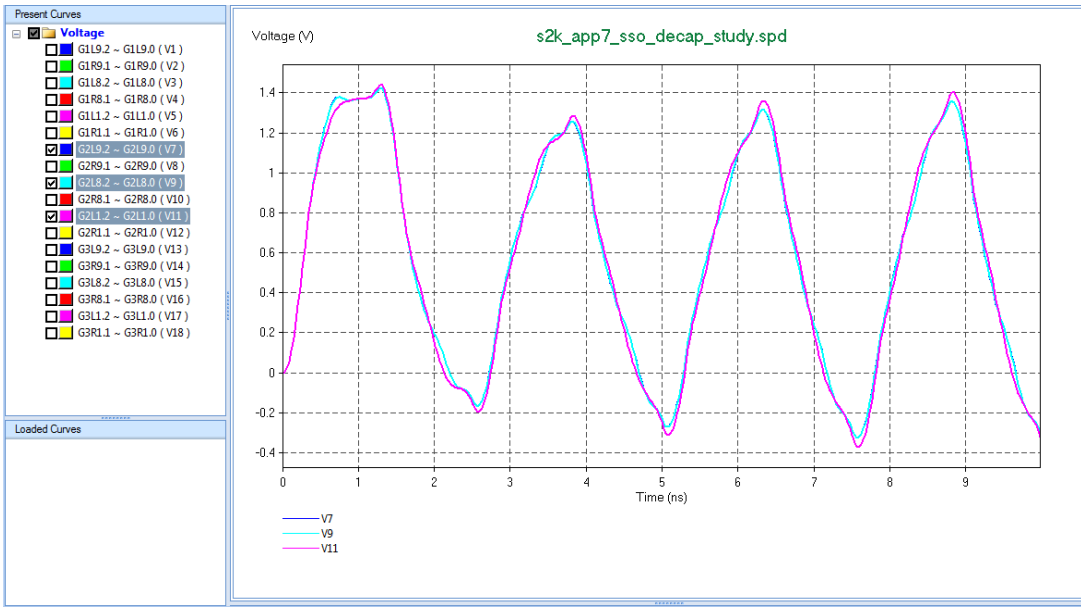
Voltage waveforms at the load end of the 1st, 8th and 9th nets are displayed in the following illustration. This drawing shows that the three curves are almost identical.



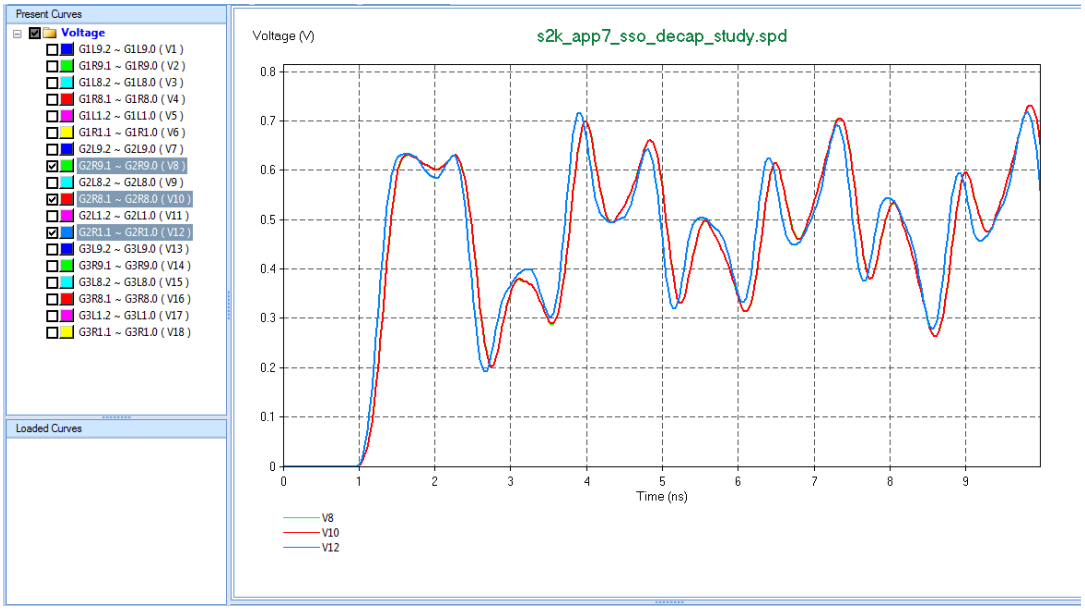
Results of the Second Group of Nets

The two illustrations in this section show that, for the 17 simultaneous nets passing planes through vias, the waveforms on the nets are severely corrupted. This can seriously affect the timing budget, since the skew can easily reach tens of ps.

Voltage waveforms at the source end of the 1st, 8th and 9th nets are displayed in the figure below.



Voltage waveforms at the load end of the 1st, 8th and 9th nets are displayed in the next illustration.



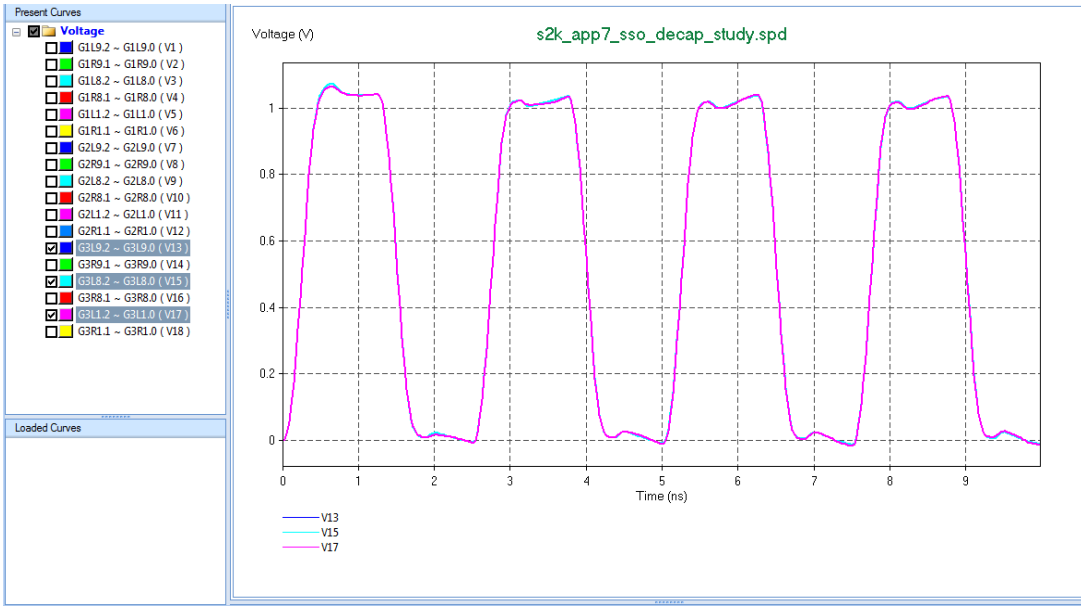
Results of the Third Group of Nets

After 72 decoupling capacitors are placed around vias on both the top and the bottom signal layers,

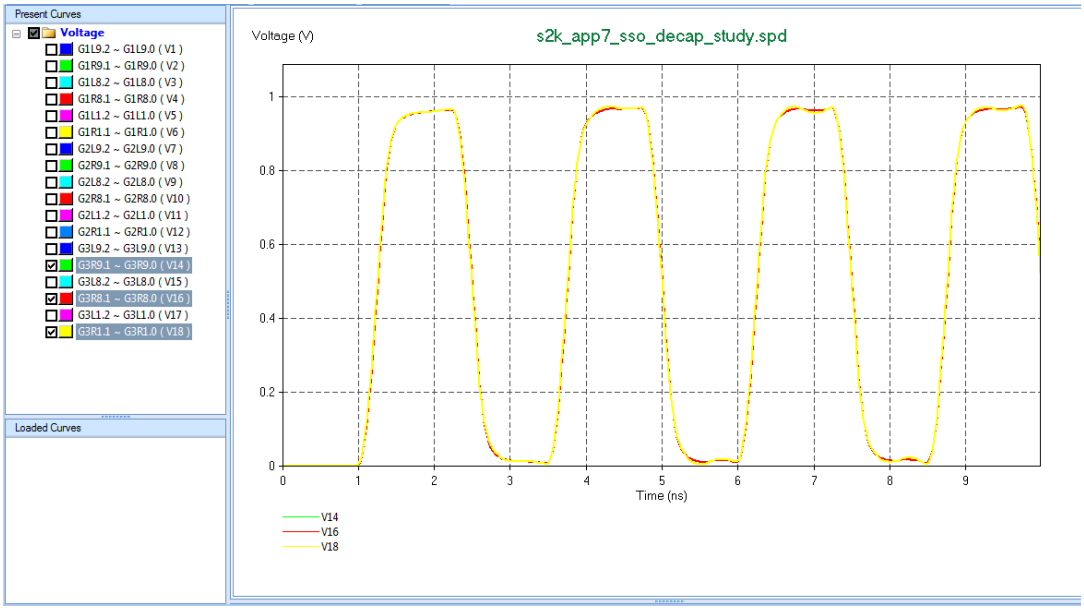
voltage waveforms at the source and load ends of the 1st, 8th and 9th nets are displayed.

The next illustration is the comparison of voltage waveforms at the source ends of the 9th net of the three net groups.

Near End Voltage Waveforms for Group 3

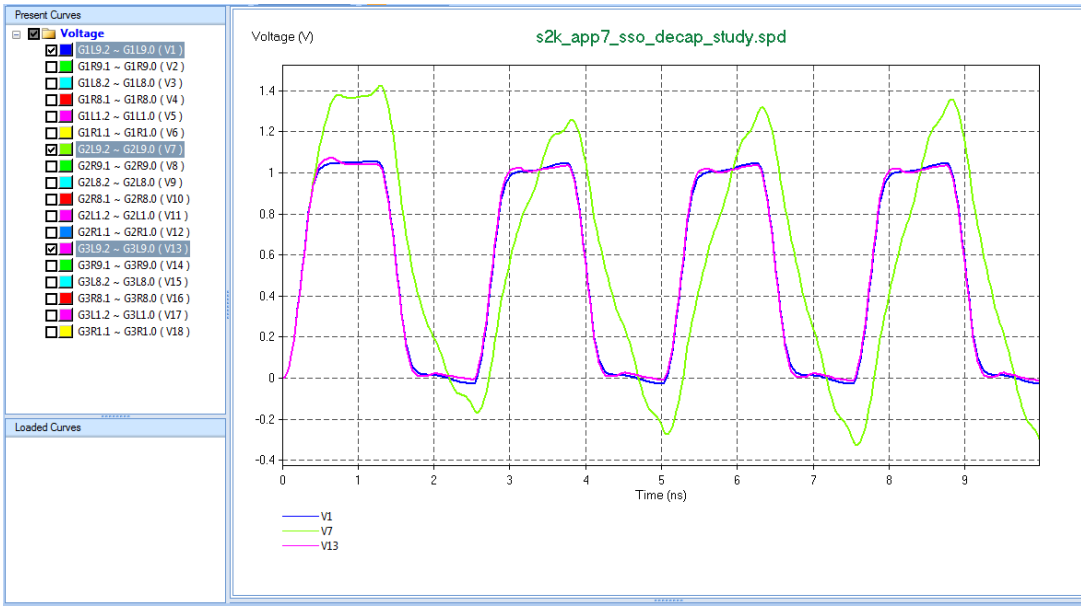


Far End Voltage Waveforms for Group 3



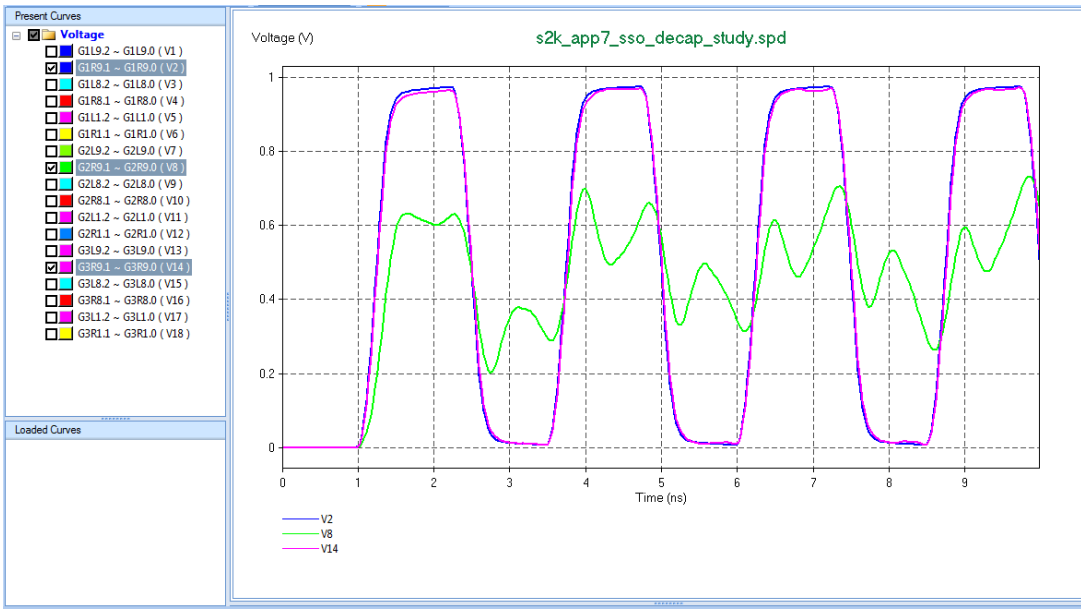
The next illustration shows the voltage waveforms at the load ends of the 9th net of the three net groups.

Near End Voltage Waveforms for Line 9 in Three Groups



From results shown in these figures, you can see that the damage in signal waveforms caused by vias is mostly recovered by the massive decoupling capacitors placed near vias.

Far End Voltage Waveforms for Line 9 in Three Groups



Index